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Circuit Level Performance of FETS: A Comparative Study of Propagation Delay with Half Adder

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Abstract: *This paper deals with the propagation delay comparison of half adder with different FETs; such as MOSFET, CNTFET, FINFET. Nanotechnology is the promising field which functions at the molecular level to replace the conventional use of classical CMOS. By simulation, the best part is got that CNTFET shows lesser delay for half adder circuit.*

Keywords: *CNTFET, MOSFET, FINFET, Hspice, Nanotechnology, propagation delay evaluation, CMOS, half adder, nanotube devices.*

I. Introduction

Popularized word "Nanotechnology" is the process, in which the arrangement of individual atoms is properly controlled by manipulating structure, length within scale of one-billionth of a meter. [3]The Nano devices can be used for efficient purposes in microelectronics, power electronics, aerospace etc.[4] Carbon nanotube field-effect transistor (CNTFET) and Fin field-effect transistor (FINFET) are very popular nano scaled transistors nowadays.[2] Propagation delay expresses certain time which is required for a signal to move from input to output and it's a major factor for a device.[11]In this paper, the simulation results will show that CNTFET has better propagation delay character with the reasons working behind it.[10]

II. Methods

In this paper, timing diagrams of CMOS based half adder circuit is shown by using Synopsys Hspice software (version 2008.03) which is an open source analog electronic circuit simulator.[5]While using MOSFET based circuits, the cell library is already existed in default list. But for simulating CNTFET and FINFET based circuits, different cell libraries and net lists have to be generated. For CNTFET library, License agreement of Stanford University is used and for FINFET library BSIM-CMG models are used which are characterized as a standard library.[6][7] It is developed by using predictive technology (PTM).[8][9] From the net lists, measured values of different points of circuits are plotted using another software Matlab which provides a numerical environment allowing programming language of fourth-generation. It shows the difference among the transistors' performance in same graphs as characteristics curves. From relative results, it is seen that propagation delay analysis of CNTFET is comparatively better than other two.[1]

III. Findings And Argument

Half adder circuit is simulated using MOSFET, CNTFET and FINFET for different netlists to examine the switching delay among those.

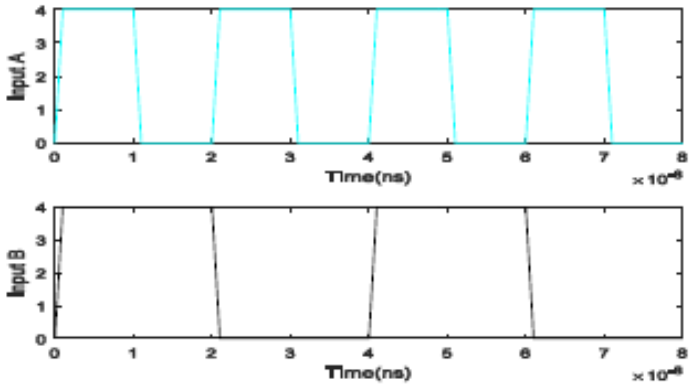

Fig. 1: The input pulses for half adder circuit

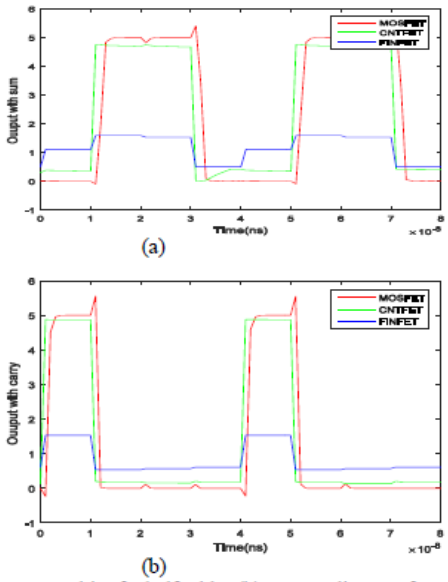

Fig. 2(a) Output diagram for a Sum bit of a half adder (b) Output diagram for a carry bit of a half adder

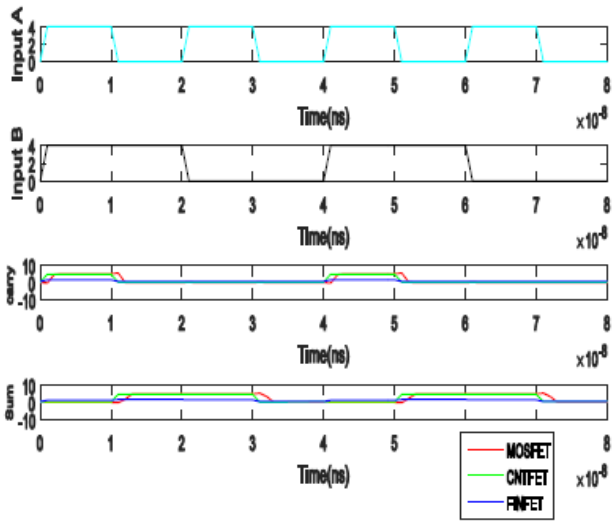

Fig. 3 Overall Timing diagram for a half Adder with different topology

In Fig. 1, Fig. 2 and Fig. 3, black and cyan colors are used to show two input signals. Red, green and blue respectively show timing diagram of MOSFET, CNTFET and FINFET. The propagation delay is symbolized by Tpd which is the summation of two parts-time delay of high to low (TpHL) and time delay of low to high (TpLH). It is measured from the difference of the instantaneous response value and the given input.

Table 1: Time delay analysis for three FETS in half adder circuit

	MOSFET	CNTFET	FINFET
For Sum	TpLH= 0.033ms TpHL= 0.067ms Total Tpd= 0.1005ms	TpLH=0ms TpHL=0ms Total Tpd=0ms	TpLH= 0ms TpHL= 0.033ms Total Tpd= 0.033ms
For Carry	TpLH= 0.1234ms TpHL= 0.067ms Total Tpd= 0.1904ms	TpLH=0ms TpHL=0ms Total Tpd=0ms	TpLH= 0.033ms TpHL= 0ms Total Tpd= 0.033ms

Propagation delay occurs for many reasons such as high voltage supply, increase in output load capacitance, operating temperature. Capacitance needs time to get charged and discharged and in both times output can't get changed instantly which is the main parameter of the delay. CNTFET and FINFET show less time delay between switching on and switching off the circuit rather than MOSFET. But comparatively CNTFET performs best because of least value of quantum capacitance which leads to lesser propagation delay.[12]

IV. Conclusion

Propagation delay determines the working speed feature of a circuit. The circuit which has less propagation delay can be considered as efficient. Nowadays the manufacturing process of CMOS is designed in nano-dimensions because of this issue. For the most efficient half adder circuit, CNTFET is the best alternative. But due to being expensive and highly controlling issue CNTFET has still some difficulties to get used widely but in nano scale regime, using CNTFET is much beneficiary.

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